WHAT IS CLAIMED IS

1. A semiconductor integrated circuit device comprising:

a control circuit for controlling a well bias of a PMOS transistor and an NMOS transistor, the control circuit being formed in a part of a region for forming a main circuit constructed mainly by a CMOS formed by the PMOS and NMOS transistors during a process of forming said main circuit,

wherein said control circuit has: means for detecting a deviation of delay time of a critical path having the longest delay time formed in said main circuit from a design parameter and determining said well bias in accordance with the deviation; and means for detecting a difference between a threshold voltage of said PMOS transistor and a threshold voltage of said NMOS transistor, and said control circuit has a function of correcting said well bias in accordance with the difference output.